## *Amendments to the Claims*

This listing of claims will replace all prior versions, and listings of claims in the application.

Claims 1-7. (Cancelled)

Claim 8. (Previously presented) A superscalar microprocessor for processing instructions having a program order, the microprocessor comprising:

a fetch circuit configured to fetch instructions, including a conditional branch instruction, from an instruction store;

a branch detection circuit configured to detect the conditional branch instruction from among the fetched instructions;

a branch bias circuit configured to receive a branch bias signal indicating whether a conditional branch controlled by the conditional branch instruction is predicted to be taken or not taken;

a stream identifier circuit configured to associate a stream identifier with one or more of the fetched instructions, thereby identifying a first stream predicted by the branch bias signal;

a buffer circuit configured to receive and buffer the fetched instructions;

a decode circuit coupled to the buffer circuit and configured to make a group of buffered instructions concurrently available for execution as decoded instructions, wherein the available decoded instructions include a decoded instruction

corresponding to the conditional branch instruction and a decoded instruction from the

first stream; and

an execution circuit including a plurality of functional units configured to

execute the available decoded instructions out of the program order, wherein execution

of the conditional branch instruction determines whether the conditional branch is taken,

wherein the fetch circuit is further configured to cancel instructions from

the first stream based on the stream identifier in the event that the branch bias signal

incorrectly predicts whether the conditional branch is taken.

Claim 9. (Previously presented) The superscalar microprocessor of claim 8,

wherein the functional units concurrently execute a first decoded instruction and a

second decoded instruction, wherein according to the program order the first decoded

instruction corresponds to an instruction that is prior to the conditional branch instruction

and the second decoded instruction corresponds to an instruction from the first stream

that is subsequent to the conditional branch instruction.

Claim 10. (Previously presented) The superscalar microprocessor of claim 8,

wherein the stream identifier comprises a stream bit.

Claim 11. (Previously presented) The superscalar microprocessor of claim 8,

wherein the stream identifier indicates an occurrence of a control flow change associated

with the conditional branch instruction.

Claim 12. (Previously presented) The superscalar microprocessor of claim 8, wherein the stream identifier is associated with a predetermined number of the fetched instructions.

Claim 13. (Previously presented) The superscalar microprocessor of claim 8, wherein the fetch circuit fetches one or more instructions of a second stream not predicted by the branch bias signal before the decoded conditional branch instruction is executed.

Claim 14. (Previously presented) The superscalar microprocessor of claim 8, further comprising a register file including a plurality of entries configured to store data including result data generated by the plurality of functional units, wherein each of the plurality of entries is accessible by reference to a respective location in the register file.

Claim 15. (Previously presented) The superscalar microprocessor of claim 8, further comprising an instruction retirement circuit configured to receive operation completion information from the plurality of functional units and to retire the executed instructions according to the program order.

Claim 16. (Previously presented) The superscalar microprocessor of claim 15 wherein the fetch circuit fetches one or more instructions of a second stream not predicted by the branch bias signal before the conditional branch instruction is retired.

Claim 17. (Previously presented) The superscalar microprocessor of claim 8, further comprising an instruction retirement circuit configured to receive result data from the plurality of functional units, the result data including branch result data associated with the conditional branch instruction, and to confirm the result data according to the program order.

Claim 18. (Previously presented) The superscalar microprocessor of claim 17, wherein the fetch circuit fetches one or more instructions of a second stream not predicted by the branch bias signal before the branch result data is confirmed by the instruction retirement circuit.

Claim 19. (Previously presented) The superscalar microprocessor of claim 8, wherein the buffer circuit is further configured to cancel instructions from the first stream based on the stream identifier in the event that the branch bias signal incorrectly predicts whether the conditional branch is taken.

Claim 20. (Previously presented) In a superscalar microprocessor, a method for processing instructions having a program order, the method comprising the steps of:

fetching instructions from an instruction store;

detecting a conditional branch instruction from among the plurality of fetched instructions;

receiving a branch bias signal associated with the conditional branch instruction, the branch bias signal indicating whether the conditional branch is predicted to be taken or not taken;

associating a stream identifier with one or more of the fetched instructions, thereby identifying a first stream predicted by the branch bias signal;

making a group of the fetched instructions concurrently available for execution, wherein the available instructions include the conditional branch instruction and an instruction from the first stream;

executing the available instructions out of the program order, wherein execution of the conditional branch instruction determines whether the conditional branch is taken;

determining, based on the execution of the conditional branch instruction, whether the branch bias signal correctly predicted whether the conditional branch is taken; and

in the event that the branch bias signal incorrectly predicted whether the conditional branch is taken, canceling instructions from the first stream based on the stream identifier.

Claim 21. (Previously presented) The method of claim 20, wherein the executing step includes concurrently executing a first instruction and a second instruction, wherein according to the program order the first instruction is prior to the conditional branch instruction and the second instruction is an instruction from the first stream that is subsequent to the conditional branch instruction.

Claim 22. (Previously presented) The method of claim 20, wherein the stream identifier comprises a stream bit.

Claim 23. (Previously presented) The method of claim 20, wherein the stream identifier indicates an occurrence of a control flow change associated with the conditional branch instruction.

Claim 24. (Previously presented) The method of claim 20, wherein the stream identifier is associated with a predetermined number of the plurality of instructions.

Claim 25. (Previously presented) The method of claim 20, wherein the fetching step further includes fetching instructions from a second stream not predicted by the branch bias signal prior to execution of the conditional branch instruction.

Claim 26. (Previously presented) The method of claim 20, further comprising the steps of:

receiving operation completion information generated during the step of executing; and

retiring the executed instructions according to the program order in response to the operation completion information,

wherein the step of fetching includes fetching instructions from a second stream not predicted by the branch bias signal prior to retiring the conditional branch instruction.

Claim 27. (Previously presented) The method of claim 20, further comprising the steps of:

receiving operation completion information and result data generated during the step of executing, the result data including branch result data generated during execution of the conditional branch instruction; and

confirming the result data according to the program order and in response to the operation completion information,

wherein the step of fetching and buffering includes fetching instructions from a second stream not predicted by the branch bias signal prior to confirming the branch result data.

Claim 28. (Previously presented) A computer system, comprising:

a memory;

a superscalar microprocessor for processing instructions having a program order; and

a bus coupled between the memory and the microprocessor,

wherein the microprocessor includes:

a fetch circuit configured to fetch instructions, including a conditional branch instruction, from an instruction store;

a branch detection circuit configured to detect the conditional branch

instruction from among the fetched instructions;

a branch bias circuit configured to receive a branch bias signal indicating

whether a conditional branch controlled by the conditional branch instruction is predicted

to be taken or not taken;

a stream identifier circuit configured to associate a stream identifier with

one or more of the fetched instructions, thereby identifying a first stream predicted by the

branch bias signal;

a buffer circuit configured to receive and buffer the fetched instructions;

a decode circuit coupled to the buffer circuit and configured to make a

group of buffered instructions concurrently available for execution as decoded

instructions, wherein the available decoded instructions include a decoded instruction

corresponding to the conditional branch instruction and a decoded instruction from the

first stream; and

an execution circuit including a plurality of functional units configured to

execute the available decoded instructions out of the program order, wherein execution

of the conditional branch instruction determines whether the conditional branch is taken,

wherein the fetch circuit is further configured to cancel instructions from

the first stream based on the stream identifier in the event that the branch bias signal

incorrectly predicts whether the conditional branch is taken.


Claim 29.  (Previously presented)  The system of claim 28, wherein the

functional units concurrently execute a first decoded instruction and a second decoded

instruction, wherein according to the program order the first decoded instruction

corresponds to an instruction that is prior to the conditional branch instruction and the

second decoded instruction corresponds to an instruction from the first stream that is

subsequent to the conditional branch instruction.

Claim 30. (Previously presented) The system of claim 28, wherein the stream

identifier comprises a stream bit.

Claim 31. (Previously presented) The system of claim 28, wherein the stream

identifier indicates an occurrence of a control flow change associated with the

conditional branch instruction.

Claim 32. (Previously presented) The system of claim 28, wherein the stream

identifier is associated with a predetermined number of the fetched instructions.

Claim 33. (Previously presented) The system of claim 28, wherein the fetch

circuit fetches one or more instructions of a second stream not predicted by the branch

bias signal before the decoded conditional branch instruction is executed.

Claim 34. (Previously presented) The system of claim 28, wherein the

microprocessor further includes a register file including a plurality of entries configured

to store data including result data generated by the plurality of functional units, wherein

each of the plurality of entries is accessible by reference to a respective location in the register file.

Claim 35. (Previously presented) The system of claim 28, wherein the microprocessor further includes an instruction retirement circuit configured to receive operation completion information from the plurality of functional units and to retire the executed instructions according to the program order.

Claim 36. (Previously presented) The system of claim 35, wherein the fetch circuit fetches one or more instructions of a second stream not predicted by the branch bias signal before the conditional branch instruction is retired.

Claim 37. (Previously presented) The system of claim 28, wherein the microprocessor further includes an instruction retirement circuit configured to receive result data from the plurality of functional units, the result data including branch result data associated with the conditional branch instruction, and to confirm the result data according to the program order.

Claim 38. (Previously presented) The system of claim 37, wherein the fetch circuit fetches one or more instructions of a second stream not predicted by the branch bias signal before the branch result data is confirmed by the instruction retirement circuit.

Claim 39. (Previously presented) The system of claim 28, wherein the buffer circuit is further configured to cancel instructions from the first stream based on the stream identifier in the event that the branch bias signal incorrectly predicts whether the conditional branch is taken.

Claim 40. (New) The superscalar microprocessor of claim 8, wherein the decode circuit is further configured to concurrently decode a plurality of instructions including a first instruction and a second instruction, wherein the second instruction has a data dependency on the first instruction.

Claim 41. (New) The method of claim 20 wherein making the group of fetched instructions concurrently available for execution includes concurrently decoding a first one and a second one of the group of the fetched instructions, wherein the second one of the instructions has a data dependency on the first one of the instructions.

Claim 42. (New) The system of claim 28, wherein the decode circuit is further configured to concurrently decode a plurality of instructions including a first instruction and a second instruction, wherein the second instructions has a data dependency on the first instruction.